	L #	Hits	Search Text	DBs
1	L1	37	(detect$3 near10 (invalid$4 near10 (instruction opcode code))).ab,ti.	USPAT; US-PGPUB
2	L2	2	((opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 (instruction near10 (select$3 replac$5 substitut$3) near10 (nop noop no-op))	EPO; JPO; DERWENT; IBM_TDB
3	L3	10	((opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 (instruction near10 (select$3 replac$5 substitut$3) near10 (nop noop no-op))	USPAT; US-PGPUB
4	L4	10	((opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 ((opcode instruction) near10 (select$3 replac$5 substitut$3) near10 (nop noop no-op))	USPAT; US-PGPUB
5	L5	155	((detect$3 determin$3 check$3 verif$6 match$3 compar$3) near10 (opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 ((opcode instruction) near10 (select$3 replac$5 substitut$3))	USPAT; US-PGPUB
6	L6	22	((detect$3 determin$3 check$3 verif$6 match$3 compar$3) near10 (opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 ((opcode instruction) near10 (select$3 replac$5 substitut$3))	EPO; JPO; DERWENT; IBM_TDB

	L #	Hits	Search Text	DBs
1	L4	9505	instruction near10 (valid$4 invalid$4 correct incorrect)	USPAT; US-PGPUB
2	L5	224	instruction near10 (select$3 replac$5 substitut$3) near10 (nop noop no-op)	USPAT; US-PGPUB
3	L6	10	4 near50 5	USPAT; US-PGPUB
4	L7	2752	instruction near10 (valid$4 invalid$4 correct incorrect)	EPO; JPO; DERWENT; IBM_TDB
5	L8	51	instruction near10 (select$3 replac$5 substitut$3) near10 (nop noop no-op)	EPO; JPO; DERWENT; IBM_TDB
6	L9	2	7 near50 8	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20020144176 A1	☐	Method and apparatus for improving reliability in microprocessors	714/11
2	US 20020144087 A1	☐	Architecture of method for fetching microprocessor's instructions	712/207
3	US 5504916 A	☐	Digital signal processor with direct data transfer from external memory	712/36
4	US 5442799 A	☐	Digital signal processor with high speed multiplier means for double data input	712/36
5	US 5421023 A	☐	Motion vector calculation method using sequential minimum distortion calculations at different densities	348/701
6	US 5408625 A	☐	Microprocessor capable of decoding two instructions in parallel	712/210
7	US 5388236 A	☐	Digital signal processor with multiway branching based on parallel evaluation of N threshold values followed by sequential evaluation of M	712/236
8	US 5243705 A	☐	System for rapid return of exceptional processing during sequence operation instruction execution	712/228
9	US 5161247 A	☐	Digital signal processor matching data blocks against a reference block and replacing the reference block when a new minimum distortion block is calculated	712/36
10	US 5031096 A	☐	Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor	711/169

	Document ID	U	Title	Current OR
1	JP 20031 14796 A	☐	COMPUTER CONTROL CIRCUIT	
2	JP 20021 96950 A	☒	DEBUGGING SYSTEM	
3	JP 20020 07113 A	☒	MICROPROCESSOR AND HOST COMPUTER AND REWRITING DEVICE	
4	JP 20012 90638 A	☒	COMPUTER SYSTEM AND INSTRUCTION EXCHANGING METHOD	
5	JP 20000 81982 A	☒	COMPILER, PROCESSOR AND RECORDING MEDIUM	
6	JP 11306 028 A	☒	INSTRUCTION CACHE CONTROLLER AND RECORDING MEDIUM	
7	JP 11288 374 A	☒	SIMULATOR FOR DIGITAL COMPUTER	
8	JP 11249 881 A	☒	CONTROLLER	
9	JP 11149 390 A	☒	DATA PROCESSOR AND FAULT DIAGNOSTIC METHOD IN THE SAME	
10	JP 10340 209 A	☒	DATA PROCESSOR	
11	JP 10254 695 A	☒	MICROPROGRAM SPEED CONTROL CIRCUIT	
12	JP 08179 945 A	☒	SIGNAL PROCESSOR	
13	JP 08069 340 A	☒	METHOD AND DEVICE FOR MEASURING NUMBER OF CLOCK CYCLE	
14	JP 07295 694 A	☒	POWER SAVING METHOD FOR ARITHMETIC PROCESSOR	
15	JP 06195 226 A	☒	PROGRAM LOADING SYSTEM	
16	JP 05334 197 A	☒	INSTRUCTION RAM UPDATING CIRCUIT	
17	JP 04361 328 A	☒	PROCESSING MODE SWITCHING SYSTEM	
18	JP 04274 520 A	☒	MICROPROGRAM CONTROLLER	
19	JP 04074 227 A	☒	OPTIMIZATION SYSTEM FOR MACHINE WORD CODE	
20	JP 02132 545 A	☒	PARALLEL COMPUTER AND ITS COMPILING METHOD	
21	JP 02081 237 A	☒	CHECKING METHOD FOR USER PROGRAM OF ONE CHIP MICROCOMPUTER	

	Document ID	U	Title	Current OR
22	JP 01253 032 A	☒	MICROPROGRAM CONTROL TYPE PROCESSOR	
23	JP 01213 719 A	☒	DATA REARRANGING DEVICE FOR PIPELINE PROCESSING	
24	JP 01211 135 A	☒	PROGRAM DEBUGGING SYSTEM	
25	JP 63137 330 A	☒	MICROPROGRAM CONTROLLER	
26	JP 63061 330 A	☒	MICROPROGRAM CONTROL DEVICE	
27	JP 62254 238 A	☒	COMPILING DEVICE	
28	JP 62010 736 A	☒	PREFETCHING CONTROL SYSTEM FOR MICRO INSTRUCTION	
29	JP 61217 838 A	☒	TEST METHOD OF MICROPROCESSOR	
30	JP 61213 929 A	☒	DATA PROCESSING DEVICE WITH AUXILIARY PROCESSOR	
31	JP 61068 640 A	☒	INSTRUCTION PROCESSING CIRCUIT OF MICROCOMPUTER	
32	JP 60105 048 A	☒	MICROPROGRAM CONTROL SYSTEM	
33	JP 57210 497 A	☒	ROM DATA INSPECTION SYSTEM	
34	JP 56169 451 A	☒	DATA TRANSMISSION SYSTEM	
35	NNRD4 10118	☒	Generic Methodology for Code Patching in Binary File	
36	NB901 1326	☒	Masked Delayed Branches for Pipelined Computer Processors.	
37	JP 20031 14796 A	☒	Computer control circuit, has selector for selecting No operation instruction code, when instruction code output from synchronous memory corresponds to jump command	
38	US 63743 46 B	☒	Instruction execution method in microprocessor in digital system, involves comparing condition value in selected condition register with two different values for executing inspection or treating instructions as NOP	
39	JP 20010 15690 A	☒	Large scale integrated system outputs initialization information corresponding to address value output by CPU to internal data bus, when selecting signal is invalid	
40	US 63145 10 B	☒	Microprocessor has decoder that decodes modified nop instruction having dirty bit register field of selected dirty bit register and generates decoded signals	
41	JP 11306 028 A	☒	Instruction cache control apparatus for memory access in reduced instruction set computer - has instruction generation unit that outputs pre-instruction to fetch and replace instruction address of predetermined line point with NOP instruction in present line	
42	JP 11249 881 A	☒	Control apparatus e.g. programmable logic controller - has NOP instruction area and substituted objective program that are superscribed by substituted program, after NOP instruction area is distributed immediately after substituted objective program	

	Document ID	U	Title	Current OR
43	EP 926596 A	☒	Instruction reordering method for reducing processor power consumption	
44	JP 11149390 A	☒	Error detection method for calculator of data processor e.g. computer - involves comparing output of calculator with previous calculation result, stored in register, using comparator which outputs error signal when compared data are different	
45	JP 10161875 A	☒	Parallel data processor with calculator fault detection function - outputs fault detection signal showing calculator failure, based on comparison of calculation results using source operand and predetermined calculator	
46	RD 410118 A	☒	Code patching for binary file e.g. for fixing Year-2000 omissions in all shipped product - locating patch code at end of code segment that requires modification, changing first instruction of original code into CALL instruction to activate patch code, and then replacing all of original code with no-operation instructions	
47	JP 09022399 A	☒	Parallel image processor with image memory and processor array - in which address of image memory designated by instruction in command latch is output to processor array, when instruction stored in command latch is memory access command	
48	JP 08179945 A	☒	Audio signal processing appts. for CD - has instruction ROM storing DSP arithmetic command, address control command, NOP command selection bit and NOP frequency display bit using which outputs of multiplier and adder are processed	
49	JP 07181969 A	☒	Code segment substitution device - has memory interface which stores new instructions in host memory after replacing current instructions into MSP memory after masking process	
50	US 5396622 A	☒	Radix sorting system using dynamic branch table - distributing contents of input bucket to several output buckets according to value of key field byte of present rank	
51	TW 207579 A	☐	Microprocessor instructions pre-read and pre-decode method - involves storing adjacent instructions in odd and even buses and setting program counter value during decoding step before execution of next instruction	

	L #	Hits	Search Text	DBs
1	L1	37	(detect$3 near10 (invalid$4 near10 (instruction opcode code))).ab,ti.	USPAT; US-PGPUB
2	L2	2	((opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 (instruction near10 (select$3 replac$5 substitut$3) near10 (nop noop no-op))	EPO; JPO; DERWENT; IBM_TDB
3	L3	10	((opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 (instruction near10 (select$3 replac$5 substitut$3) near10 (nop noop no-op))	USPAT; US-PGPUB
4	L4	10	((opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 ((opcode instruction) near10 (select$3 replac$5 substitut$3) near10 (nop noop no-op))	USPAT; US-PGPUB
5	L6	22	((detect$3 determin$3 check$3 verif$6 match$3 compar$3) near10 (opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 ((opcode instruction) near10 (select$3 replac$5 substitut$3))	EPO; JPO; DERWENT; IBM_TDB
6	L5	155	((detect$3 determin$3 check$3 verif$6 match$3 compar$3) near10 (opcode instruction) near10 (valid$4 invalid$4 correct incorrect)) near50 ((opcode instruction) near10 (select$3 replac$5 substitut$3))	USPAT; US-PGPUB
7	L12	58	(detect$3 near10 (invalid$4 near10 (instruction opcode))).ab,ti.	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20030190078 A1	☐	Apparatus and method for detecting error in a digital image	382/232
2	US 20030095521 A1	☐	Device, system, method and computer readable medium for pairing of devices in a short distance wireless network	370/338
3	US 20020071491 A1	☐	Signal processor	375/240.23
4	US 20020070863 A1	☐	Tagging system and method	340/572.1
5	US 6441810 B1	☐	Telemetry encoding technique for smart stylus	345/179
6	US 6178495 B1	☐	Processor E-unit to I-unit interface instruction modification with E-unit opcode computer logic in the unit	712/209
7	US 6154504 A	☐	Encoding method, encoding apparatus, decoding method, decoding apparatus, and recording medium	375/265
8	US 6131088 A	☐	Electronic catalog system and method	705/27
9	US 6092185 A	☐	Opcode compare logic in E-unit for breaking infinite loops, detecting invalid opcodes and other exception checking	712/219
10	US 5961633 A	☐	Execution of data processing instructions	712/216
11	US 5881279 A	☐	Method and apparatus for handling invalid opcode faults via execution of an event-signaling micro-operation	712/244
12	US 5850532 A	☐	Invalid instruction scan unit for detecting invalid predecode data corresponding to instructions being fetched	712/213
13	US 5822313 A	☐	Seamless handover in a cordless TDMA system	370/332
14	US 5802076 A	☐	Audio error mitigation technique for a TDMA communication system	714/747
15	US 5754864 A	☐	Software piracy detection system	717/173
16	US 5745504 A	☐	Bit error resilient variable length code	714/752
17	US 5687311 A	☐	Microcomputer with detection of predetermined data for enabling execution of instructions for stopping supply of clock	714/34
18	US 5671231 A	☐	Method and apparatus for performing cache snoop testing on a cache system	714/724
19	US 5649137 A	☐	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
20	US 5612884 A	☐	Remote meter operation	705/403
21	US 5550837 A	☐	Adaptive differential pulse code modulation system with transmission error compensation	714/708

	Document ID	U	Title	Current OR
22	US 5542084 A	☐	Method and apparatus for executing an atomic read-modify-write instruction	345/501
23	US 5511175 A	☐	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
24	US 5404557 A	☐	Data processor with plural instruction execution parts for synchronized parallel processing and exception handling	712/23
25	US 5369401 A	☐	Remote meter operation	705/403
26	US 5365048 A	☐	Bar code symbol reading apparatus with double-reading preventing function	235/462.08
27	US 5226130 A	☐	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/238
28	US 4890253 A	☐	Predetermination of result conditions of decimal operations	708/525
29	US 4809087 A	☐	Apparatus for recording a discriminative signal	386/100
30	US 4799255 A	☐	Communication facilities access control arrangement	379/189
31	US 4646167 A	☐	Time code decoder	386/62
32	US 4581488 A	☐	Last number redial device	379/359
33	US 4508939 A	☐	Last number redial device	379/357.04
34	US 4241396 A	☐	Tagged pointer handling apparatus	711/154
35	US 4167778 A	☐	Invalid instruction code detector	712/208
36	US 3940762 A	☐	Digital detection criteria control device for video mapping, detection parameter control, optimum radar receiver selection and rejection of non-moving targets	342/90
37	US 3770900 A	☐	AUDIO MULTIFREQUENCY SIGNAL RECEIVER	379/351

	Document ID	U	Title	Current OR
1	US 20030 18254 0 A1	☐	Method for limiting physical resource usage in a virtual tag allocation environment of a microprocessor	712/225
2	US 20030 18253 7 A1	☒	Mechanism to assign more logical load/store tags than available physical registers in a microprocessor system	712/216
3	US 20030 17225 8 A1	☒	Control forwarding in a pipeline digital processor	712/234
4	US 20030 14398 1 A1	☒	Sequential presentation of long instructions in an interactive voice response system	455/414 .1
5	US 20030 13135 1 A1	☒	Video system for integrating observer feedback with displayed images	725/24
6	US 20030 13122 0 A1	☒	Bi-directional return register stack recovery from speculative execution of call/return upon branch misprediction	712/242
7	US 20030 10594 3 A1	☒	Mechanism for processing speclative LL and SC instructions in a pipelined processor	712/216
8	US 20030 09377 1 A1	☒	Debugging aid device, a compiling device, a debugging aid program, a compiling program, and a computer readable record medium therefor	717/125
9	US 20030 09249 2 A1	☒	Game system, game control method, and recording medium for the same	463/42
10	US 20030 07006 2 A1	☒	System and method for reducing computing system latencies associated with branch instructions	712/234
11	US 20030 04385 8 A1	☒	Device for processing data signals, method thereof, and device for multiplexing data signals	370/537
12	US 20030 03722 5 A1	☒	Apparatus and method for microcontroller debugging	712/227
13	US 20020 18883 4 A1	☒	Apparatus and method for target address replacement in speculative branch target address cache	712/238
14	US 20020 15708 4 A1	☒	Method and system for displaying translation information	717/141
15	US 20020 15199 2 A1	☒	Media recording device with packet data interface	700/83
16	US 20020 12416 2 A1	☒	Computer system and method for fetching a next instruction	712/238
17	US 20020 10429 3 A1	☒	Packaging system	53/472

	Document ID	U	Title	Current OR
18	US 20020095459 A1	☒	Method and apparatus for providing a client by a server with an instruction data set in a predetermined format in response to a content data request message by a client	709/203
19	US 20020083312 A1	☒	Branch Prediction apparatus and process for restoring replaced branch history for use in future branch predictions for an executing program	712/240
20	US 20020069375 A1	☒	System, method, and article of manufacture for data transfer across clock domains	713/400
21	US 20020030751 A1	☒	Image control device with information-based image correcting capability, image control method and digital camera	348/222.1
22	US 20020010851 A1	☒	Emulated branch effected by trampoline mechanism	712/244
23	US 20010018764 A1	☒	Method and apparatus for translating between source and target code	717/146
24	US 20010016941 A1	☒	Method for translating between source and target code with heterogenous register sets	717/141
25	US 20010016940 A1	☒	System and method for translating include files	717/141
26	US 20010016870 A1	☒	Method for at least making ready for mailing at least one message, and data structure for use therein	709/203
27	US 20010013086 A1	☒	Multiprocessor system and data transmitting method	711/119
28	US 6631460 B1	☒	Advanced load address table entry invalidation based on register address wraparound	712/217
29	US 6594821 B1	☒	Translation consistency checking for modified target instructions by comparing to original copy	717/136
30	US 6560696 B1	☒	Return register stack target predictor	712/237
31	US 6550002 B1	☒	Method and system for detecting a flush of an instruction without a flush indicator	712/216
32	US 6550001 B1	☒	Method and implementation of statistical detection of read after write and write after write hazards	712/216
33	US 6513109 B1	☒	Method and apparatus for implementing execution predicates in a computer processing system	712/200
34	US 6505296 B2	☒	Emulated branch effected by trampoline mechanism	712/244
35	US 6477641 B2	☒	Method for translating between source and target code with heterogenous register sets	712/241
36	US 6477639 B1	☒	Branch instruction mechanism for processor	712/237

	Document ID	U	Title	Current OR
37	US 6457175 B1	☒	Method and apparatus for installing a software upgrade within a memory resource associated with a computer system	717/173
38	US 6456777 B1	☒	Information processor, information processing method and information recording medium on which information processing method is recorded	386/46
39	US 6446197 B1	☒	Two modes for executing branch instructions of different lengths and use of branch control instruction and register set loaded with target instructions	712/237
40	US 6418424 B1	☒	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system	706/21
41	US 6400996 B1	☒	Adaptive pattern recognition based control system and method	700/83
42	US 6389531 B1	☒	Indexing branch target instruction memory using target address generated by branch control instruction to reduce branch latency	712/237
43	US 6374370 B1	☒	Method and system for flexible control of BIST registers based upon on-chip events	714/39
44	US 6374348 B1	☒	Prioritized pre-fetch/preload mechanism for loading and speculative preloading of candidate branch target instruction	712/237
45	US 6356997 B1	☒	Emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system	712/237
46	US 6324643 B1	☒	Branch prediction and target instruction control for processor	712/237
47	US 6308258 B1	☒	Data processing circuit with target instruction and prefix instruction	712/210
48	US 6304961 B1	☒	Computer system and method for fetching a next instruction	712/238
49	US 6272561 B1	☒	Sound blaster interface card auto-detection method	710/8
50	US 6253374 B1	☒	Method for validating a signed program prior to execution time or an unsigned program at execution time	717/126
51	US 6253317 B1	☒	Method and apparatus for providing and handling traps	712/244
52	US 6247123 B1	☒	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239
53	US 6185676 B1	☒	Method and apparatus for performing early branch prediction in a microprocessor	712/239
54	US 6185674 B1	☒	Method and apparatus for reconstructing the address of the next instruction to be completed in a pipelined processor	712/230
55	US 6167505 A	☒	Data processing circuit with target instruction and prefix instruction	712/210
56	US 6167460 A	☒	System for replacing control information in a printer according to external instruction information if a replacement function is valid	710/5
57	US 6081750 A	☒	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system	700/17
58	US 6077312 A	☒	Apparatus, program product and method of debugging utilizing a context sensitive breakpoint	717/129
59	US 6059840 A	☒	Automatic scheduling of instructions to reduce code size	717/154

	Document ID	U	Title	Current OR
60	US 6059225 A	☒	Flight control device for an aircraft, in particular a helicopter	244/17.13
61	US 6049860 A	☒	Pipelined floating point stores	712/25
62	US 6035426 A	☒	System for memory error checking in an executable	714/54
63	US 6033074 A	☒	Subjective eye refractive power measuring apparatus	351/212
64	US 6023561 A	☒	System for processing traceable cache trace information	714/45
65	US 6014728 A	☒	Organization of an integrated cache unit for flexible usage in supporting multiprocessor operations	711/133
66	US 6012125 A	☒	Superscalar microprocessor including a decoded instruction cache configured to receive partially decoded instructions	711/125
67	US 6009539 A	☒	Cross-triggering CPUs for enhanced test operations in a multi-CPU computer system	714/30
68	US 6003107 A	☒	Circuitry for providing external access to signals that are internal to an integrated circuit chip package	710/316
69	US 5983337 A	☒	Apparatus and method for patching an instruction by providing a substitute instruction or instructions from an external memory responsive to detecting an opcode of the instruction	712/32
70	US 5974543 A	☒	Apparatus and method for performing subroutine call and return operations	712/240
71	US 5964869 A	☒	Instruction fetch mechanism with simultaneous prediction of control-flow instructions	712/236
72	US 5964862 A	☒	Execution unit and method for using architectural and working register files to reduce operand bypasses	712/23
73	US 5956477 A	☒	Method for processing information in a microprocessor to facilitate debug and performance monitoring	714/30
74	US 5956476 A	☒	Circuitry and method for detecting signal patterns on a bus using dynamically changing expected patterns	714/30
75	US 5949972 A	☒	System for memory error checking in an executable	714/54
76	US 5948098 A	☒	Execution unit and method for executing performance critical and non-performance critical arithmetic instructions in separate pipelines	712/221
77	US 5940074 A	☒	Remote upgrade of software over a network	345/749
78	US 5935238 A	☒	Selection from multiple fetch addresses generated concurrently including predicted and actual target by control-flow instructions in current and previous instruction bundles	712/206
79	US 5923862 A	☒	Processor that decodes a multi-cycle instruction into single-cycle micro-instructions and schedules execution of the micro-instructions	712/208
80	US 5920890 A	☒	Distributed tag cache memory system and method for storing data in the same	711/144
81	US 5901246 A	☒	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system	382/209

	Document ID	U	Title	Current OR
82	US 5887243 A	☒	Signal processing apparatus and methods	725/136
83	US 5887003 A	☒	Apparatus and method for comparing a group of binary fields with an expected pattern to generate match results	714/736
84	US 5881279 A	☒	Method and apparatus for handling invalid opcode faults via execution of an event-signaling micro-operation	712/244
85	US 5881224 A	☒	Apparatus and method for tracking events in a microprocessor that can retire more than one instruction during a clock cycle	714/47
86	US 5881217 A	☒	Input comparison circuitry and method for a programmable state machine	714/30
87	US 5880671 A	☒	Flexible circuitry and method for detecting signal patterns on a bus	340/146.2
88	US 5875108 A	☒	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system	700/17
89	US 5872947 A	☒	Instruction classification circuit configured to classify instructions into a plurality of instruction types prior to decoding said instructions	712/213
90	US 5867644 A	☒	System and method for on-chip debug support and performance monitoring in a microprocessor	714/39
91	US 5848433 A	☒	Way prediction unit and a method for operating the same	711/137
92	US 5764946 A	☒	Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address	712/239
93	US 5764624 A	☒	Aim switching system and path changing method	370/218
94	US 5748978 A	☒	Byte queue divided into multiple subqueues for optimizing instruction selection logic	712/23
95	US 5740418 A	☒	Pipelined processor carrying out branch prediction by BTB	712/239
96	US 5737749 A	☒	Method and system for dynamically sharing cache capacity in a microprocessor	711/123
97	US 5729707 A	☒	Instruction prefetch circuit and cache device with branch detection	712/207
98	US 5717587 A	☒	Method and system for recording noneffective instructions within a data processing system	700/2
99	US 5644779 A	☒	Processing system and method of operation for concurrent processing of branch instructions with cancelling of processing of a branch instruction	712/23
100	US 5627992 A	☒	Organization of an integrated cache unit for flexible usage in supporting microprocessor operations	711/133
101	US 5619408 A	☒	Method and system for recoding noneffective instructions within a data processing system	712/226
102	US 5581774 A	☒	Data processor decoding and executing a train of instructions of variable length at increased speed	712/210
103	US 5548739 A	☒	Method and apparatus for rapidly retrieving data from a physically addressed data storage structure using address page crossing predictive annotations	711/204

	Document ID	U	Title	Current OR
104	US 5535405 A	☒	Microsequencer bus controller system	710/110
105	US 5524224 A	☒	System for speculatively executing instructions wherein mispredicted instruction is executed prior to completion of branch processing	712/219
106	US 5500942 A	☒	Method of indicating parallel execution compoundability of scalar instructions based on analysis of presumed instructions	712/210
107	US 5479616 A	☒	Exception handling for prefetched instruction bytes using valid bits to identify instructions that will cause an exception	712/212
108	US 5455938 A	☒	Network based machine instruction generator for design verification	716/5
109	US 5440696 A	☒	Data processing device for reducing the number of internal bus lines	710/305
110	US 5432849 A	☒	Secure cryptographic operations using control vectors generated inside a cryptographic facility	380/280
111	US 5408625 A	☒	Microprocessor capable of decoding two instructions in parallel	712/210
112	US 5355461 A	☒	Method of and apparatus for selecting an origin address for use in translating a logical address in one of a plurality of virtual address spaces to a real address in a real address space	711/203
113	US 5353426 A	☒	Cache miss buffer adapted to satisfy read requests to portions of a cache fill in progress without waiting for the cache fill to complete	711/118
114	US 5353421 A	☒	Multi-prediction branch prediction mechanism	712/240
115	US 5335277 A	☒	Signal processing appparatus and methods	380/242
116	US 5319362 A	☒	Security system with security access database distributed among individual access devices	340/5.33
117	US 5297255 A	☒	Parallel computer comprised of processor elements having a local memory and an enhanced data transfer mechanism	712/14
118	US 5289588 A	☒	Interlock acquisition for critical code section execution in a shared memory common-bus individually cached multiprocessor system	711/120
119	US 5283873 A	☒	Next line prediction apparatus for a pipelined computed system	712/207
120	US 5276853 A	☒	Cache system	711/131
121	US 5243705 A	☒	System for rapid return of exceptional processing during sequence operation instruction execution	712/228
122	US 5233654 A	☒	Signal processing apparatus and methods	725/135
123	US 5222122 A	☒	Payphone having master and slave modes	379/32.04
124	US 5206823 A	☒	Apparatus to perform Newton iterations for reciprocal and reciprocal square root	708/502
125	US 5185878 A	☒	Programmable cache memory as well as system incorporating same and method of operating programmable cache memory	711/123

	Document ID	U	Title	Current OR
126	US 5167026 A	☒	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
127	US 5148528 A	☒	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
128	US 5142633 A	☒	Preprocessing implied specifiers in a pipelined processor	712/225
129	US 5136691 A	☒	Methods and apparatus for caching interlock variables in an integrated cache memory	711/139
130	US 5129075 A	☒	Data processor with on-chip logical addressing and off-chip physical addressing	711/169
131	US 5109414 A	☒	Signal processing apparatus and methods	725/135
132	US 5075849 A	☒	Information processor providing enhanced handling of address-conflicting instructions during pipeline processing	711/200
133	US 5031096 A	☒	Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor	711/169
134	US 5025366 A	☒	Organization of an integrated cache unit for flexible usage in cache system design	711/128
135	US 4972317 A	☒	Microprocessor implemented data processing system capable of emulating execution of special instructions not within the established microprocessor instruction set by switching access from a main store portion of a memory	712/227
136	US 4965825 A	☒	Signal processing apparatus and methods	380/233
137	US 4827402 A	☒	Branch advanced control apparatus for advanced control of a branch instruction in a data processing system	712/234
138	US 4800563 A	☒	Error processing method and apparatus for information processing system	714/6
139	US 4791557 A	☒	Apparatus and method for monitoring and controlling the prefetching of instructions by an information processing system	712/244
140	US 4665501 A	☒	Workstation for local and remote data processing	710/8
141	US 4642771 A	☒	Diagnostic processing system for automatic transmission of an automobile	701/62
142	US 4628093 A	☒	Code reading operations supervisor	235/375
143	US 4617625 A	☒	Vector processor	712/4
144	US 4531198 A	☒	Operation mode monitor for microcomputer	714/23
145	US 4524415 A	☒	Virtual machine data processor	714/21
146	US 4488228 A	☒	Virtual memory data processor	714/21
147	US 4418333 A	☒	Appliance control system	340/310.01

	Document ID	U	Title	Current OR
148	US 4408554 A	☒	Automatic needle thread control apparatus	112/302
149	US 4368534 A	☒	Keyboard controlled vital digital communication system	714/807
150	US 4231089 A	☒	Data processing system with apparatus for correcting microinstruction errors	714/7
151	US 4210785 A	☒	Tape replay system	360/72.2
152	US 4176460 A	☒	Opto-mechanical measuring system	33/504
153	US 4136383 A	☒	Microprogrammed, multipurpose processor having controllable execution speed	712/221
154	US 3944986 A	☒	Vehicle movement control system for railroad terminals	104/88.04
155	US 3851152 A	☐	READ-OUT DATA ENTRY SYSTEM FOR A PLURALITY OF SUPER-IMPOSED DATA ENTRY CARDS	235/435

	Document ID	U	Title	Current OR
1	JP 20022 43279 A	☐	COMBUSTION CONTROLLER	
2	JP 20011 68772 A	☒	DEVICE AND METHOD FOR SWITCHING HOT STANDBY LINE	
3	JP 20011 54877 A	☒	DEVICE AND METHOD FOR CONTROLLING INTERRUPTION	
4	JP 10083 301 A	☒	PARALLEL PROCESSOR	
5	JP 07200 294 A	☒	PROCESSOR DEVICE PROVIDED WITH DELAY BRANCH EXECUTION FUNCTION	
6	JP 06168 263 A	☒	VECTOR PROCESSOR	
7	JP 06110 784 A	☒	MICROPROCESSOR DEVICE	
8	JP 06095 862 A	☒	INSTRUCTION STRING OPTIMIZATION SUPPORTING DEVICE	
9	JP 06095 614 A	☒	DISPLAY DEVICE	
10	JP 05346 890 A	☒	DATA INVALIDATION CONTROL SYSTEM	
11	JP 05224 930 A	☒	DATA PROCESSOR PROVIDED WITH PLURAL INSTRUCTION EXECUTING PARTS	
12	JP 04333 928 A	☒	LSI CONTROL SYSTEM	
13	JP 04324 193 A	☒	ELECTRICALLY PROGAMMABLE READ ONLY MEMORY ATTACHED WITH WRITE PROTECTION	
14	JP 04182 735 A	☒	INFORMATION PROCESSOR	
15	JP 04177 440 A	☒	DATA PROCESSOR	
16	JP 04081 959 A	☒	INPUT/OUTPUT INSTRUCTION CONTROL SYSTEM	
17	JP 04055 940 A	☒	MICROPROGRAM CONTROL SYSTEM	
18	JP 04025 953 A	☒	CACHE MEMORY ERROR PROCESSING SYSTEM	
19	JP 03296 111 A	☒	OPERATION CONTROLLER FOR UNMANNED CARRIER	
20	JP 03211 622 A	☒	INFORMATION PROCESSOR	
21	JP 03209 523 A	☒	DETECTION SYSTEM FOR ERROR OF INSTRUCTION DATA	
22	JP 03142 533 A	☒	CHECK SYSTEM FOR DECIMAL DATA	

	Document ID	U	Title	Current OR
23	JP 03095 676 A	☒	BACK-UP DEVICE FOR VERIFICATION OF SIMULATION RESULT	
24	JP 02235 151 A	☒	DETECTING/CORRECTING SYSTEM FOR INVALID DATA IN PROGRAM EXECUTION	
25	JP 02208 743 A	☒	DATA PROCESSOR	
26	JP 02029 850 A	☒	TIGHT COUPLING PROCESSORS	
27	JP 01307 851 A	☒	STORAGE CONTROL SYSTEM	
28	JP 01224 739 A	☒	MICROCAMERA	
29	JP 01193 939 A	☒	SYSTEM FOR CONTROLLING INSTRUCTION FETCH	
30	JP 01076 353 A	☒	CONTROL SYSTEM FOR INPUT/OUTPUT INSTRUCTION	
31	JP 63244 153 A	☒	MEMORY PROTECTING METHOD	
32	JP 63070 343 A	☒	MICROCOMPUTER	
33	JP 63026 088 A	☒	VIDEO FLOPPY REPRODUCING DEVICE	
34	JP 61294 553 A	☒	INSTRUCTION PROCESSING SYSTEM	
35	JP 61015 235 A	☒	CENTRAL PROCESSOR	
36	JP 60083 149 A	☒	COMPUTER	
37	JP 58035 647 A	☒	APPRECIATING DEVICE FOR MICROCOMPUTER	
38	GB 22822 45 A	☒	Aborting execution of instructions.	
39	EP 34336 3 A2	☒	Motor control system.	
40	US 65429 87 B	☒	Instruction queue status detection method in pipelined computer architecture, involves subtracting number of enqueued instructions from sum of number of free rows and issued instructions, to determine number of free rows in specific cycle	
41	GB 23790 57 A	☒	Memory operations testing method for computer program development detects accesses to unmapped region of two-region virtual memory associated with physical memory	
42	US 61192 04 A	☒	Translation lookaside buffer coherency maintenance involves continuing processing of instructions in interval between receipt of synchronization request and sending of indication to first processor	
43	US 58812 79 A	☒	Invalid opcode fault handling method for reduced instruction set (RISC) microprocessors used in computer system	

	Document ID	U	Title	Current OR
44	US 5850532 A	☒	Invalid instruction scanner for superscalar microprocessor - has invalid instruction scan unit that detects invalid predecode information and identifies specific byte through invalid instruction pointer	
45	JP 10322411 A	☒	Data communication control apparatus for motor vehicle - has invalid processors provided for received data, which include control instructions for other apparatuses in motor vehicle, when latch signal and clock signal are not detected	
46	US 5668984 A	☒	Floating point processing system - detecting if operand is in valid form while being loaded into pipeline, staging execution of instruction when operand is invalid, converting operand to valid form, and using gate to present converted operand to pipeline after one delay stag	
47	US 5479616 A	☒	Exception handling system for prefetched instruction bytes in pipelined 486-type microprocessor - stores prefetched instruction byte in queue with valid bit if byte is invalid, when exception occurs, and detects if stall condition results from exception associated with prefetched instruction byte by checking stored instruction status	
48	JP 07252031 A	☒	Hall call registration device for lift system - has multiplication scene call button which registers call based on detected guest, and invalidates prior instruction after lift door opens at correct floor	
49	JP 07200294 A	☒	Pipeline processor with delay branch execution function - has command execution unit that executes delay branch instruction after completion of exception processing started by exception processing unit	
50	US 5404557 A	☒	Data processor - has instruction execution parts for synchronised parallel processing which generates order of each group of instructions having successive addresses and order of each instruction in each group of instructions	
51	EP 721619 B	☒	Processing appts. for data stored in RAM - has conditional controller responding to memory access and condition test circuitry to prevent completion of current instruction on instruction error	
52	EP 469239 A	☒	Detection and correction appts. for faulty processor operational codes - detects faulty instructions using logic nor circuit and replaces them with error-free micro-code from programmable array	
53	US 5226130 A	☒	Branch prediction cache with maintained consistency - organises store into instruction stream detection resulting in invalidation of corresponding cache entry data and main memory access	
54	US 4942525 A	☒	Data processor for concurrent executing of instructions - comprises instruction control circuit for decoding M instructions and reading operands in parallel, detection circuit and reserve circuit	
55	EP 155275 B	☒	Data processor with instruction execution unit - has n-stage pipeline for providing data segments representing instruction words from memory to execution unit	
56	EP 981694 A	☒	Data processing system providing performance measurement - uses interruption of timer for triggering performance measurement and stores results of processing of each measurement item	
57	EP 663764 A	☒	Data processing system with instruction buffer - pre-transfers instructions from main storage to buffer which is invalidated only when changed content is executed as instruction	
58	US 4167778 A	☐	Invalid instruction code detector for digital computer - has RAM with flag indicating whether a particular combination of operation code bits is valid	

	Document ID	U	Title	Current OR
1	JP 20023 14519 A	☐	BIT SYNCHRONIZING CIRCUIT	
2	JP 20002 98587 A	☒	PROCESSOR HAVING DEVICE BRANCHED TO SPECIFIED PARTY DURING INSTRUCTION REPETITION	
3	JP 10228 399 A	☒	PARTIAL FILE UPDATING DEVICE	
4	JP 08137 687 A	☒	PROGRAM CONTROLLER	
5	JP 06089 174 A	☒	COMPUTER MEMORY SYSTEM	
6	JP 05127 720 A	☒	OFFLINE INSTRUCTION DEVICE FOR ROBOT	
7	JP 05035 175 A	☒	EDUCATIONAL SYSTEM	
8	JP 04283 856 A	☒	DOCUMENT PROCESSOR	
9	JP 62242 104 A	☒	CONTROL DEVICE FOR RUNNING OIL HYDRAULIC MOTOR	
10	JP 57209 547 A	☒	COLLECTING DEVICE FOR PROGRAM EXECUTING CARRIER INFORMATION	
11	EP 23902 3 A1	☒	Arrangement for processing branch instructions in pipelined data-processing systems.	
12	JP 20031 86663 A	☒	Data processing system determines content to be corrected based on content transfer instructions and compares corrected content with selected data so as to notify correction completion state	
13	US 64053 07 B	☒	Self modifying code conflict handling method in microprocessor, involves invalidating selected portion of information progressing through front end of IVE pipeline when contents of SAB matches with instruction pointer	
14	US 62725 61 B	☒	Sound blaster interface card auto-detection method, involves identifying detection of card to be successfully completed on receiving an interruption	
15	GB 23453 54 A	☒	Method of sound card interface auto detection	
16	US 56194 08 A	☒	Instruction processing method for data processing system of superscalar, pipelined microprocessor - involves determining if selected instruction would be noneffective if executed by processor, and dispatching it to completion buffer if it does or recoding selected instruction, prior to dispatch to execution unit, if it does not	
17	EP 71636 4 A	☒	Operator running support system for large scale e.g. nuclear, thermal or hydraulic power plant - compares guidance data operation instructions with selected output operation instructions to evaluate their correctness, with selected operation instructions being sent as control output when correct	
18	EP 46923 9 A	☒	Detection and correction appts. for faulty processor operational codes - detects faulty instructions using logic nor circuit and replaces them with error-free micro-code from programmable array	
19	WO 91037 80 A	☒	Controlling robot to prevent vibration in tip of its mechanism - determining current instruction value by adding correction torque found in selected operation expression to torque instruction value	

	Document ID	U	Title	Current OR
20	EP 306209 A	☒	Dual rail processors with error checking at single rail interfaces - has shared resource devices coupled to processors for receiving data from output instructions from processors simultaneously	
21	US 4488228 A	☒	Virtual memory data processor - stores information relating to internal state upon detection of access fault during instruction execution	
22	JP 58182113 A	☐	Signal compensating device in decoding of digital signal - can selectively change instruction signal providing appropriate correction depending on detected burst length. NoAbstract Dwg 0/6	